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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,392	08/06/2003	Mohammad Shahabuddin	CIT.PAU.40	1184

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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 10/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,392	SHAHABUDDIN ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 have been examined and rejected.

Priority

2. Applicants' claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. The provisional application number is 60/405,110, filed August 21, 2002.

Drawings

3. The drawings are objected to for the following reasons. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include **all** of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the Examiner, the Applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3-1. In Figure 1, reference number 107 should be associated with "Test Master".

3-2. It appears that "Increment k by 1", as shown in step 406 of Figure 41, should be "Increment K by 1".

Specification

4. The disclosure is objected to because of the following informalities. Appropriate correction is required.

4-1. As described in line 2 of page 2, "Ingredient #4, on of the most important". (Emphasis added).

4-2. It appears that "upon receiving a command form the master launcher submodule", as described in lines 7-8 of page 7, should be "upon receiving a command from the master launcher submodule".

4-3. It appears that "identical to blocks 201, 202, 203, 204, and 206 in Fig. 2 respectively", as described in lines 22-23 of page 12, should be "identical to blocks 201, 202, 203, 204, 205, and 206 in Fig. 2 respectively".

Claim Objections

5. Claims 7 and 20 are objected to because of the following informalities. Appropriate correction is required.

5-1. Regarding claim 7, "upon receiving a command form the master launcher submodule", as described in line 3 of the claim. (Emphasis added.)

5-2. Regarding claim 20, "upon receiving a command form the master launcher submodule", as described in lines 2-3 of the claim. (Emphasis added.)

Recommendations

6. Claim 9 recites the limitations "the slave deployment" in line 3 of the claim. For clarification purpose, the Examiner suggests that "the slave deployment" be replaced with "the slave deployment submodule".

7. Claim 22 recites the limitations "running the slave deployment at the workstation" in lines 2-3 of the claim. For clarification purpose, the Examiner suggests that "running the slave deployment at the workstation" be replaced with "running the slave deployment submodule at the workstation".

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Hellestrand et al., U.S. Patent 6,230,114 B1 issued May 8, 2001

9-1. Regarding claim 1, Hellestrand et al. disclose a virtual real time system for simulating a physical test environment comprising:

A master computer module (the interface mechanism, column 14, lines 36-43); and

at least one slave computer module communicated to the master computer module and having a clocked operation, which is synchronized to the master computer module (processor1 simulator 208, FIG. 2);

wherein the master computer module and at least one each slave computer module each have a launcher submodule (the kernel in the interface mechanism, column 14, lines 36-43) and a deployment submodule (hardware simulator 203, FIG. 2), the launcher submodule for launching the deployment submodule and controlling the deployment submodule for synchronized operation with the master computer module, the deployment submodule generating a virtual clock and following commands from the launcher submodule (each processor simulator has its own concept of time, as does the hardware simulator, column 8, lines 51-57).

9-2. Regarding claim 2, Hellestrand et al. further disclose where the launcher submodule in the master computer module is a central virtual real time controller for the system (simulation time is started and maintained by the hardware simulator, column 9, lines 58-63).

9-3. Regarding claim 3, Hellestrand et al. further disclose where the deployment submodule in the master computer module generates a virtual clock signal based on process CPU instruction execution (The hardware simulator provides the simulation time frame, column 19, lines 13-15).

9-4. Regarding claim 4, Hellestrand et al. further disclose where the system includes an operating system and where the launcher submodule and the deployment submodule in the master computer module and in the slave computer module communicate via signals provided by the operating system (using a complete or partial operating system, column 8, lines 48-50).

9-5. Regarding claim 5, Hellestrand et al. further disclose comprising a test master computer submodule communicating with the master launcher submodule for configuring the system and advancing, starting, stopping, adjusting and monitoring virtual real time, and/or issuing time related commands to the deployment submodule in the master computer module (the simulation is run under debugger control, column 15, line 64, through column 16, line 2).

9-6. Regarding claim 6, Hellestrand et al. further disclose where the master deployment submodule generates a virtual clock signal and where test master computer submodule generates scale-up and/or scale-down commands of the virtual clock in the master deployment submodule (Any units of time may be used, column 19, lines 13-15).

9-7. Regarding claim 7, Hellestrand et al. further disclose where the slave launcher submodule further comprises a slave launcher synch submodule and where the slave launcher submodule, upon receiving a command from the master launcher submodule (a start signal in the digital circuitry starts the processor simulator for processor 1, column 19, lines 15-26), requests the corresponding slave deployment submodule via the slave launcher synch submodule to advance the slave deployment submodule by a predetermined number of virtual clock ticks and to stop (Processor 1 executes for a time $\Delta T2$ until T3, column 19, lines 15-26), after which the slave deployment submodule suspends operation and waits for the slave launcher submodule to resume operation (to suspend operation of processor simulator 207, column 19, lines 15-26),.

9-8. Regarding claim 8, Hellestrand et al. further disclose where master launcher submodule sends a start-tick command to only to the slave launcher submodule, if it is prepared to receive the next start-tick command by sending a socket call with a start-tick message (a start signal in the digital circuitry starts the processor simulator for processor 1, column 19, lines 15-26).

9-9. Regarding claim 9, Hellestrand et al. further disclose where the slave deployment submodule master deployment submodule each run and are included in a workstation, and where the slave deployment submodule is not running at the workstation where the master deployment submodule is running (carrying out the simulation in a host computer system that includes several host processors interconnected using a network connection, column 11, lines 22-58).

9-10. Regarding claim 10, Hellestrand et al. further disclose where the slave launcher submodule after receiving a start-tick command from the master deployment submodule sends a SIGCONT signal to the suspended slave deployment submodule (a start signal in the digital circuitry starts the processor simulator for processor 1, column 19, lines 15-26), the slave launcher submodule sends an acknowledgment message to the master launcher submodule, the slave deployment submodule in parallel with other programs runs the requested number of ticks (Processor 1 executes for a time $\Delta T2$ until T3, column 19, lines 15-26).

9-11. Regarding claim 11, Hellestrand et al. further disclose where the master launcher submodule then sends a signal SIGCONT to its corresponding master deployment submodule to run a requested number of virtual clock ticks based on Vclk clock ticks which are generated when the time consumed by execution of process CPU instructions is equal to or greater than tick-resolution time, the master deployment submodule suspends its operation after running the requested number and the master launcher submodule waits for the master deployment submodule to complete its cycles (The waitEvent function waits for the occurrence of any event or time out on the given delay, column 17, lines 35-40).

9-12. Regarding claim 12, Hellestrand et al. further disclose where the master launcher submodule sends a stop-tick message to each slave launcher submodule which needs to be synchronized at that clock tick based on slave tick synchronize size and a stop-tick socket call is made to the candidate slave launcher submodule (a library of functions is provided ... to affect synchronizations, column 16, lines 18-35).

9-13. Regarding claim 13, Hellestrand et al. further disclose where the slave launcher submodule after receiving a stop-tick command waits for a SIGSTOP signal from the slave

deployment submodule to make sure that the requested number of virtual clock ticks has been completed, and the slave launcher submodule sends a stop-tick acknowledgment message to the master launcher submodule (The asynchronous event handler function is called when an asynchronous event occurs, column 18, lines 25-39).

9-14. Regarding claims 14-26, these method claims include equivalent limitations as in claims 1-13 and are anticipated using the same analysis of claims 1-13.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to Applicants' disclosure.

Reference to Bortfeld, U.S. Patent 6,993,469 B1 issued January 31, 2006, and filed June 2, 2000, is cited as disclosing a method for unified simulation.

11. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day
September 18, 2006 H.D.

KAMINI SHAH
SUPERVISORY PATENT EXAMINER